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KEY=CADENCE - EVIE ARMSTRONG

FPGAS FOR SOFTWARE PROGRAMMERS

Springer This book makes powerful Field Programmable Gate Array (FPGA) and reconfigurable technology accessible to software engineers by covering different state-of-the-art high-level synthesis approaches (e.g., OpenCL and several C-to-gates compilers). It introduces FPGA technology, its programming model, and how various applications can be implemented on FPGAs without going through low-level hardware design phases. Readers will get a realistic sense for problems that are suited for FPGAs and how to implement them from a software designer’s point of view. The authors demonstrate that FPGAs and their programming model reflect the needs of stream processing problems much better than traditional CPU or GPU architectures, making them well-suited for a wide variety of systems, from embedded systems performing sensor processing to large setups for Big Data number crunching. This book serves as an invaluable tool for software designers and FPGA design engineers who are interested in high design productivity through behavioural synthesis, domain-specific compilation, and FPGA overlays. Introduces FPGA technology to software developers by giving an overview of FPGA programming models and design tools, as well as various application examples; Provides a holistic analysis of the topic and enables developers to tackle the architectural needs for Big Data processing with FPGAs; Explains the reasons for the energy efficiency and performance benefits of FPGA processing; Provides a user-oriented approach and a sense for where and how to apply FPGA technology.

HANDBOOK OF RESEARCH ON ADVANCED HYBRID INTELLIGENT TECHNIQUES AND APPLICATIONS

IGI Global Conventional computational methods, and even the latest soft computing paradigms, often fall short in their ability to offer solutions to many real-world problems due to uncertainty, imprecision, and circumstantial data. Hybrid intelligent computing is a paradigm that addresses these issues to a considerable extent. The Handbook of Research on Advanced Hybrid Intelligent Techniques and Applications highlights the latest research on various issues relating to the hybridization of artificial intelligence, practical applications, and best methods for implementation. Focusing on key interdisciplinary computational intelligence research dealing with soft computing techniques, pattern mining, data analysis, and computer vision, this book is relevant to the research needs of academics, IT specialists, and graduate-level students.

TRANSACTION-LEVEL POWER MODELING

Springer This book describes for readers a methodology for dynamic power estimation, using Transaction Level Modeling (TLM). The methodology exploits the existing tools for RTL simulation, design synthesis and SystemC prototyping to provide fast and accurate power estimation using Transaction Level Power Modeling (TLPM). Readers will benefit from this innovative way of evaluating power on a high level of abstraction, at an early stage of the product life cycle, decreasing the number of the expensive design iterations.

SYNTHESIS METHODOLOGY FOR BUILT-IN AT-SPEED TESTING

HIGH PERFORMANCE EMBEDDED ARCHITECTURES AND COMPILERS

THIRD INTERNATIONAL CONFERENCE, HIPEAC 2008, GÖTEBORG, SWEDEN, JANUARY 27-29, 2008, PROCEEDINGS

Springer Science & Business Media This highly relevant and up-to-the-minute book constitutes the refereed proceedings of the Third International Conference on High Performance Embedded Architectures and Compilers, HiPEAC 2008, held in Göteborg, Sweden, January 27-29, 2008. The 25 revised full papers presented together with 1 invited keynote paper were carefully reviewed and selected from 77 submissions. The papers are organized into topical sections on a number of key subjects in the field.

EMBEDDED SYSTEMS HANDBOOK

EMBEDDED SYSTEMS DESIGN AND VERIFICATION

CRC Press Considered a standard industry resource, the Embedded Systems Handbook provided researchers and technicians with the authoritative information needed to launch a wealth of diverse applications, including those in automotive electronics, industrial automated systems, and building automation and control. Now a new resource is required to report on current developments and provide a technical reference for those looking to move the field forward yet again. Divided into two volumes to accommodate this growth, the Embedded Systems Handbook, Second Edition presents a comprehensive view on this area of computer engineering with a currently appropriate emphasis on developments in networking and applications. Those experts directly involved in the creation and evolution of the ideas and technologies presented offer tutorials, research surveys, and technology overviews that explore cutting-edge developments and deployments and identify potential trends. This first self-contained volume of the handbook, Embedded Systems Design and Verification, is divided into three sections. It begins with a brief introduction to embedded systems design and verification. It then provides a comprehensive overview of embedded processors and various aspects of system-on-chip and FPGA, as

well as solutions to design challenges. The final section explores power-aware embedded computing, design issues specific to secure embedded systems, and web services for embedded devices. Those interested in taking their work with embedded systems to the network level should complete their study with the second volume: Network Embedded Systems.

EMBEDDED SYSTEMS HANDBOOK 2-VOLUME SET

CRC Press During the past few years there has been an dramatic upsurge in research and development, implementations of new technologies, and deployments of actual solutions and technologies in the diverse application areas of embedded systems. These areas include automotive electronics, industrial automated systems, and building automation and control. Comprising 48 chapters and the contributions of 74 leading experts from industry and academia, the Embedded Systems Handbook, Second Edition presents a comprehensive view of embedded systems: their design, verification, networking, and applications. The contributors, directly involved in the creation and evolution of the ideas and technologies presented, offer tutorials, research surveys, and technology overviews, exploring new developments, deployments, and trends. To accommodate the tremendous growth in the field, the handbook is now divided into two volumes. New in This Edition: Processors for embedded systems Processor-centric architecture description languages Networked embedded systems in the automotive and industrial automation fields Wireless embedded systems Embedded Systems Design and Verification Volume I of the handbook is divided into three sections. It begins with a brief introduction to embedded systems design and verification. The book then provides a comprehensive overview of embedded processors and various aspects of system-on-chip and FPGA, as well as solutions to design challenges. The final section explores power-aware embedded computing, design issues specific to secure embedded systems, and web services for embedded devices. Networked Embedded Systems Volume II focuses on selected application areas of networked embedded systems. It covers automotive field, industrial automation, building automation, and wireless sensor networks. This volume highlights implementations in fast-evolving areas which have not received proper coverage in other publications. Reflecting the unique functional requirements of different application areas, the contributors discuss inter-node communication aspects in the context of specific applications of networked embedded systems.

VLSI DESIGN AND TEST

21ST INTERNATIONAL SYMPOSIUM, VDAT 2017, ROORKEE, INDIA, JUNE 29 – JULY 2, 2017, REVISED SELECTED PAPERS

Springer This book constitutes the refereed proceedings of the 21st International Symposium on VLSI Design and Test, VDAT 2017, held in Roorkee, India, in June/July 2017. The 48 full papers presented together with 27 short papers were carefully reviewed and selected from 246 submissions. The papers were organized in topical sections named: digital design; analog/mixed signal; VLSI testing; devices and technology; VLSI architectures; emerging technologies and memory; system design; low power design and test; RF circuits; architecture and CAD; and design verification.

HANDBOOK OF RESEARCH ON GREEN ICT: TECHNOLOGY, BUSINESS AND SOCIAL PERSPECTIVES

TECHNOLOGY, BUSINESS AND SOCIAL PERSPECTIVES

IGI Global "This handbook coalesces worldwide investigations, thoughts, and practices in the area of Green ICT, covering the technical advances, methodological innovations, and social changes that result in enhancements and improvements in business strategies, social policies, and technical implementations"--Provided by publisher.

ENERGY-EFFICIENT COMMUNICATION PROCESSORS

DESIGN AND IMPLEMENTATION FOR EMERGING WIRELESS SYSTEMS

Springer Science & Business Media This book describes a new design approach for energy-efficient, Domain-Specific Instruction set Processor (DSIP) architectures for the wireless baseband domain. The innovative techniques presented enable co-design of algorithms, architectures and technology, for efficient implementation of the most advanced technologies. To demonstrate the feasibility of the author’s design approach, case studies are included for crucial functionality of advanced wireless systems with increased computational performance, flexibility and reusability. Designers using this approach will benefit from reduced development/product costs and greater scalability to future process technology nodes.

EFFICIENT DESIGN OF VARIATION-RESILIENT ULTRA-LOW ENERGY DIGITAL PROCESSORS

Springer This book enables readers to achieve ultra-low energy digital system performance. The author’s main focus is the energy consumption of microcontroller architectures in digital (sub)-systems. The book covers a broad range of topics extensively: from circuits through design strategy to system architectures. The result is a set of techniques and a context to realize minimum energy digital systems. Several prototype silicon implementations are discussed, which put the proposed techniques to the test. The achieved results demonstrate an extraordinary combination of variation-resilience, high speed performance and ultra-low energy.

INTEGRATED CIRCUIT AND SYSTEM DESIGN. POWER AND TIMING MODELING, OPTIMIZATION AND SIMULATION

21ST INTERNATIONAL WORKSHOP, PATMOS 2011, MADRID, SPAIN, SEPTEMBER 26-29, 2011, PROCEEDINGS

Springer This book constitutes the refereed proceedings of the 21st International Conference on Integrated Circuit and System Design, PATMOS 2011, held in Madrid, Spain, in September 2011. The 34 revised full papers presented were carefully reviewed and selected from numerous submissions. The paper feature emerging challenges in methodologies and tools for the design of upcoming generations of integrated circuits and systems and focus especially on timing, performance and power consumption as well as

architectural aspects with particular emphasis on modeling, design, characterization, analysis and optimization.

LIGHTWEIGHT CRYPTOGRAPHY FOR SECURITY AND PRIVACY

2ND INTERNATIONAL WORKSHOP, LIGHTSEC 2013, GEBZE, TURKEY, MAY 6-7, 2013, REVISED SELECTED PAPERS

Springer This book constitutes the proceedings of the 2th International Workshop on Lightweight Cryptography for Security and Privacy, LightSec 2013, held in Gebze, Turkey, during May 6-7, 2013. The 10 full papers presented together with 3 invited talks were carefully reviewed and selected from 27 submissions. The papers are grouped in topical sections on efficient Implementations and designs, block cipher cryptanalysis, wireless sensor networks, and cryptographic protocols.

APPLIED RECONFIGURABLE COMPUTING

15TH INTERNATIONAL SYMPOSIUM, ARC 2019, DARMSTADT, GERMANY, APRIL 9–11, 2019, PROCEEDINGS

Springer This book constitutes the proceedings of the 15th International Symposium on Applied Reconfigurable Computing, ARC 2019, held in Darmstadt, Germany, in April 2019. The 20 full papers and 7 short papers presented in this volume were carefully reviewed and selected from 52 submissions. In addition, the volume contains 1 invited paper. The papers were organized in topical sections named: Applications; partial reconfiguration and security; image/video processing; high-level synthesis; CGRAs and vector processing; architectures; design frameworks and methodology; convolutional neural networks.

CONSTRUCTIVE SIDE-CHANNEL ANALYSIS AND SECURE DESIGN

THIRD INTERNATIONAL WORKSHOP, COSADE 2012, DARMSTADT, GERMANY, MAY 3-4, 2012. PROCEEDINGS

Springer This book constitutes the refereed proceedings of the Third International Workshop on Constructive Side-Channel Analysis and Secure Design, COSADE 2012, held in Darmstadt, Germany, May 2012. The 16 revised full papers presented together with two invited talks were carefully reviewed and selected from 49 submissions. The papers are organized in topical sections on practical side-channel analysis; secure design; side-channel attacks on RSA; fault attacks; side-channel attacks on ECC; different methods in side-channel analysis.

PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON SOFT COMPUTING SYSTEMS

ICSCS 2015, VOLUME 1

Springer The book is a collection of high-quality peer-reviewed research papers presented in International Conference on Soft Computing Systems (ICSCS 2015) held at Noorul Islam Centre for Higher Education, Chennai, India. These research papers provide the latest developments in the emerging areas of Soft Computing in Engineering and Technology. The book is organized in two volumes and discusses a wide variety of industrial, engineering and scientific applications of the emerging techniques. It presents invited papers from the inventors/originators of new applications and advanced technologies.

HARDWARE ORIENTED AUTHENTICATED ENCRYPTION BASED ON TWEAKABLE BLOCK CIPHERS

Springer Nature This book presents the use of tweakable block ciphers for lightweight authenticated encryption, especially applications targeted toward hardware acceleration where such efficient schemes have demonstrated competitive performance and strong provable security with large margins. The first part of the book describes and analyzes the hardware implementation aspects of state-of-the-art tweakable block cipher-based mode ΘCB3. With this approach, a framework for studying a class of tweakable block cipher-based schemes is developed and two family of authenticated encryption algorithms are designed for the lightweight standardization project initiated by the National Institute of Standards and Technology (NIST): Romulus and Remus. The Romulus family is a finalist for standardization and targets a wide range of applications and performance trade-offs which will prove interesting to engineers, hardware designers, and students who work in symmetric key cryptography.

ICCAP 2021

PROCEEDINGS OF THE FIRST INTERNATIONAL CONFERENCE ON COMBINATORIAL AND OPTIMIZATION, ICCAP 2021, DECEMBER 7-8 2021, CHENNAI, INDIA

European Alliance for Innovation This proceeding constitutes the thoroughly refereed proceedings of the 1st International Conference on Combinatorial and Optimization, ICCAP 2021, December 7-8, 2021. This event was organized by the group of Professors in Chennai. The Conference aims to provide the opportunities for informal conversations, have proven to be of great interest to other scientists and analysts employing these mathematical sciences in their professional work in business, industry, and government. The Conference continues to promote better understanding of the roles of modern applied mathematics, combinatorics, and computer science to acquaint the investigator in each of these areas with the various techniques and algorithms which are available to assist in his or her research. We selected 257 papers were carefully reviewed and selected from 741 submissions. The presentations covered multiple research fields like Computer Science, Artificial Intelligence, internet technology, smart health care etc., brought the discussion on how to shape optimization methods around human and social needs.

DESIGN BASED RESEARCH

ACADEMIC PUBLICATIONS AND CITATIONS

Self Author Impact

INFORMATION SECURITY THEORY AND PRACTICE: SECURITY AND PRIVACY OF MOBILE DEVICES IN WIRELESS COMMUNICATION

5TH IFIP WG 11.2 INTERNATIONAL WORKSHOP, WISTP 2011, HERAKLION, CRETE, GREECE, JUNE 1-3, 2011, PROCEEDINGS

Springer This volume constitutes the refereed proceedings of the 5th IFIP WG 11.2 International Workshop on Information Security Theory and Practices: Security and Privacy of Mobile Devices in Wireless Communication, WISTP 2011, held in Heraklion, Crete, Greece, in June 2011. The 19 revised full papers and 8 short papers presented together with a keynote speech were carefully reviewed and selected from 80 submissions. They are organized in topical sections on mobile authentication and access control, lightweight authentication, algorithms, hardware implementation, security and cryptography, security attacks and measures, security attacks, security and trust, and mobile application security and privacy.

ADVANCES IN SIGNAL PROCESSING AND COMMUNICATION

SELECT PROCEEDINGS OF ICSC 2018

Springer This book is a collection of selected peer-reviewed papers presented at the International Conference on Signal Processing and Communication (ICSC 2018). It covers current research and developments in the fields of communications, signal processing, VLSI circuits and systems, and embedded systems. The book offers in-depth discussions and analyses of latest problems across different sub-fields of signal processing and communications. The contents of this book will prove to be useful for students, researchers, and professionals working in electronics and electrical engineering, as well as other allied fields.

HIGH-SPEED DECODERS FOR POLAR CODES

Springer A new class of provably capacity achieving error-correction codes, polar codes are suitable for many problems, such as lossless and lossy source coding, problems with side information, multiple access channel, etc. The first comprehensive book on the implementation of decoders for polar codes, the authors take a tutorial approach to explain the practical decoder implementation challenges and trade-offs in either software or hardware. They also demonstrate new trade-offs in latency, throughput, and complexity in software implementations for high-performance computing and GPGPUs, and hardware implementations using custom processing elements, full-custom application-specific integrated circuits (ASICs), and field-programmable-gate arrays (FPGAs). Presenting a good overview of this research area and future directions, High-Speed Decoders for Polar Codes is perfect for any researcher or SDR practitioner looking into implementing efficient decoders for polar codes, as well as students and professors in a modern error correction class. As polar codes have been accepted to protect the control channel in the next-generation mobile communication standard (5G) developed by the 3GPP, the audience includes engineers who will have to implement decoders for such codes and hardware engineers designing the backbone of communication networks.

SCALABLE MULTI-CORE ARCHITECTURES

DESIGN METHODOLOGIES AND TOOLS

Springer Science & Business Media As Moore’s law continues to unfold, two important trends have recently emerged. First, the growth of chip capacity is translated into a corresponding increase of number of cores. Second, the parallelization of the computation and 3D integration technologies lead to distributed memory architectures. This book describes recent research that addresses urgent challenges in many-core architectures and application mapping. It addresses the architectural design of many core chips, memory and data management, power management, design and programming methodologies. It also describes how new techniques have been applied in various industrial case studies.

DIGITAL LOGIC DESIGN USING VERILOG

CODING AND RTL SYNTHESIS

Springer This book is designed to serve as a hands-on professional reference with additional utility as a textbook for upper undergraduate and some graduate courses in digital logic design. This book is organized in such a way that that it can describe a number of RTL design scenarios, from simple to complex. The book constructs the logic design story from the fundamentals of logic design to advanced RTL design concepts. Keeping in view the importance of miniaturization today, the book gives practical information on the issues with ASIC RTL design and how to overcome these concerns. It clearly explains how to write an efficient RTL code and how to improve design performance. The book also describes advanced RTL design concepts such as low-power design, multiple clock-domain design, and SOC-based design. The practical orientation of the book makes it ideal for training programs for practicing design engineers and for short-term vocational programs. The contents of the book will also make it a useful read for students and hobbyists.

VLSI DESIGN AND TEST

23RD INTERNATIONAL SYMPOSIUM, VDAT 2019, INDORE, INDIA, JULY 4–6, 2019, REVISED SELECTED PAPERS

Springer This book constitutes the refereed proceedings of the 23st International Symposium on VLSI Design and Test, VDAT 2019,

held in Indore, India, in July 2019. The 63 full papers were carefully reviewed and selected from 199 submissions. The papers are organized in topical sections named: analog and mixed signal design; computing architecture and security; hardware design and optimization; low power VLSI and memory design; device modelling; and hardware implementation.

DEBUGGING SYSTEMS-ON-CHIP

COMMUNICATION-CENTRIC AND ABSTRACTION-BASED TECHNIQUES

Springer This book describes an approach and supporting infrastructure to facilitate debugging the silicon implementation of a System-on-Chip (SOC), allowing its associated product to be introduced into the market more quickly. Readers learn step-by-step the key requirements for debugging a modern, silicon SOC implementation, nine factors that complicate this debugging task, and a new debug approach that addresses these requirements and complicating factors. The authors' novel communication-centric, scan-based, abstraction-based, run/stop-based (CSAR) debug approach is discussed in detail, showing how it helps to meet debug requirements and address the nine, previously identified factors that complicate debugging silicon implementations of SOCs. The authors also derive the debug infrastructure requirements to support debugging of a silicon implementation of an SOC with their CSAR debug approach. This debug infrastructure consists of a generic on-chip debug architecture, a configurable automated design-for-debug flow to be used during the design of an SOC, and customizable off-chip debugger software. Coverage includes an evaluation of the efficiency and effectiveness of the CSAR approach and its supporting infrastructure, using six industrial SOCs and an illustrative, example SOC model. The authors also quantify the hardware cost and design effort to support their approach.

ASIC DESIGN AND SYNTHESIS

RTL DESIGN USING VERILOG

Springer Nature This book describes simple to complex ASIC design practical scenarios using Verilog. It builds a story from the basic fundamentals of ASIC designs to advanced RTL design concepts using Verilog. Looking at current trends of miniaturization, the contents provide practical information on the issues in ASIC design and synthesis using Synopsys DC and their solution. The book explains how to write efficient RTL using Verilog and how to improve design performance. It also covers architecture design strategies, multiple clock domain designs, low-power design techniques, DFT, pre-layout STA and the overall ASIC design flow with case studies. The contents of this book will be useful to practicing hardware engineers, students, and hobbyists looking to learn about ASIC design and synthesis.

TLM-DRIVEN DESIGN AND VERIFICATION METHODOLOGY

Lulu.com This book describes a comprehensive SystemC TLM-driven IP design and verification solution'including methodology guidelines, high-level synthesis, and TLM-aware verification basedon Cadence products'that will help designers transition to a TLM-driven design andverification flow.

DESIGN AND DEVELOPMENT OF EFFICIENT ENERGY SYSTEMS

John Wiley & Sons There is not a single industry which will not be transformed by machine learning and Internet of Things (IoT). IoT and machine learning have altogether changed the technological scenario by letting the user monitor and control things based on the prediction made by machine learning algorithms. There has been substantial progress in the usage of platforms, technologies and applications that are based on these technologies. These breakthrough technologies affect not just the software perspective of the industry, but they cut across areas like smart cities, smart healthcare, smart retail, smart monitoring, control, and others. Because of these "game changers," governments, along with top companies around the world, are investing heavily in its research and development. Keeping pace with the latest trends, endless research, and new developments is paramount to innovate systems that are not only user-friendly but also speak to the growing needs and demands of society. This volume is focused on saving energy at different levels of design and automation including the concept of machine learning automation and prediction modeling. It also deals with the design and analysis for IoT-enabled systems including energy saving aspects at different level of operation. The editors and contributors also cover the fundamental concepts of IoT and machine learning, including the latest research, technological developments, and practical applications. Valuable as a learning tool for beginners in this area as well as a daily reference for engineers and scientists working in the area of IoT and machine technology, this is a must-have for any library.

INFORMATION SECURITY TECHNOLOGY FOR APPLICATIONS

16TH NORDIC CONFERENCE ON SECURITY IT SYSTEMS, NORDSEC 2011, TALINN, ESTONIA, 26-28 OCTOBER 2011, REVISED SELECTED PAPERS

Springer This book constitutes the refereed proceedings of the 16th International Conference on Secure IT Systems, NordSec 2011, held in Tallinn, Estonia, October 26-28, 2011. The 16 revised papers presented together with 2 invited talks were carefully reviewed and selected from 51 submissions. The papers are organized in topical sections on applied cryptography, commercial security policies and their enforcement, communication and network security, security modeling and metrics, economics, law and social aspects of security, and software security and malware.

BLOCKS, TOWARDS ENERGY-EFFICIENT, COARSE-GRAINED RECONFIGURABLE ARCHITECTURES

Springer Nature This book describes a new, coarse-grained reconfigurable architecture (CGRA), called Blocks, and puts it in the context of computer architectures, and in particular of other CGRAs. The book starts with an extensive evaluation of historic and existing CGRAs and their strengths and weaknesses. This also leads to a better understanding and new definition of what

distinguishes CGRAs from other architectural approaches. The authors introduce Blocks as unique due to its separate programmable control and data paths, allowing light-weight instruction decode units to be arbitrarily connected to one or more functional units (FUs) over a statically configured interconnect. The discussion includes an explanation of how to model architectures, resulting in an area and energy model for Blocks. The accuracy of this model is evaluated against fully implemented architectures, showing that although it is three orders of magnitude faster than synthesis the error margin is very acceptable. The book concludes with a case study on a real System-on-Chip, including a RISC architecture, the Blocks CGRA and peripherals.

3D-TV SYSTEM WITH DEPTH-IMAGE-BASED RENDERING

ARCHITECTURES, TECHNIQUES AND CHALLENGES

Springer Science & Business Media Riding on the success of 3D cinema blockbusters and advances in stereoscopic display technology, 3D video applications have gathered momentum in recent years. 3D-TV System with Depth-Image-Based Rendering: Architectures, Techniques and Challenges surveys depth-image-based 3D-TV systems, which are expected to be put into applications in the near future. Depth-image-based rendering (DIBR) significantly enhances the 3D visual experience compared to stereoscopic systems currently in use. DIBR techniques make it possible to generate additional viewpoints using 3D warping techniques to adjust the perceived depth of stereoscopic videos and provide for auto-stereoscopic displays that do not require glasses for viewing the 3D image. The material includes a technical review and literature survey of components and complete systems, solutions for technical issues, and implementation of prototypes. The book is organized into four sections: System Overview, Content Generation, Data Compression and Transmission, and 3D Visualization and Quality Assessment. This book will benefit researchers, developers, engineers, and innovators, as well as advanced undergraduate and graduate students working in relevant areas.

COMMUNICATION AND SIGNAL PROCESSING

EXTENDED PAPERS

Walter de Gruyter GmbH & Co KG The book elaborates selected, extended and peer reviewed papers on Communication and Signal Proceesing. As Vol. 8 of the series on "Advances on Signals, Systems and Devices" it presents main topics such as: content based video retrieval, wireless communication systems, biometry and medical imaging, adaptive and smart antennae.

APPLIED CRYPTOGRAPHY AND NETWORK SECURITY

11TH INTERNATIONAL CONFERENCE, ACNS 2013, BANFF, AB, CANADA, JUNE 25-28, 2013. PROCEEDINGS

Springer This book constitutes the refereed proceedings of the 11th International Conference on Applied Cryptography and Network Security, ACNS 2013, held in Banff, Canada, in June 2013. The 33 revised full papers included in this volume were carefully reviewed and selected from 192 submissions. They are organized in topical sections on Cloud Cryptography; Secure Computation; Hash Function and Block Cipher; Signature; System Attack; Secure Implementation - Hardware; Secure Implementation - Software; Group-oriented Systems; Key Exchange and Leakage Resilience; Cryptographic Proof; Cryptosystems.

INNOVATIONS IN ELECTRICAL AND ELECTRONIC ENGINEERING

PROCEEDINGS OF ICEEE 2020

Springer Nature The book is a compilation of selected papers from 2020 International Conference on Electrical and Electronics Engineering (ICEEE 2020) held in National Power Training Institute HQ (Govt. of India) on February 21 – 22, 2020. The work focuses on the current development in the fields of electrical and electronics engineering like power generation, transmission and distribution, renewable energy sources and technology, power electronics and applications, robotics, artificial intelligence and IoT, control, and automation and instrumentation, electronics devices, circuits and systems, wireless and optical communication, RF and microwaves, VLSI, and signal processing. The book is beneficial for readers from both academia and industry.

SMART CARD RESEARCH AND ADVANCED APPLICATIONS

10TH IFIP WG 8.8/11.2 INTERNATIONAL CONFERENCE, CARDIS 2011, LEUVEN, BELGIUM, SEPTEMBER 14-16, 2011, REVISED SELECTED PAPERS

Springer This book constitutes the thoroughly refereed post-conference proceedings of the 10th IFIP WG 8.8/11.2 International Conference on Smart Card Research and Advanced Applications, CARDIS 2011, held in Leuven, Belgium, in September 2011. The 20 revised full papers presented were carefully reviewed and selected from 45 submissions. The papers are organized in topical sections on smart cards system security, invasive attacks, new algorithms and protocols, implementations and hardware security, non-invasive attacks, and Java card security.

PROGRESS IN VLSI DESIGN AND TEST

16TH INTERNATIONAL SYMPOSIUM ON VSLI DESIGN AND TEST, VDAT 2012, SHIPUR, INDIA, JULY 1-4, 2012, PROCEEDINGS

Springer This book constitutes the refereed proceedings of the 16th International Symposium on VSLI Design and Test, VDAT 2012, held in Shibpur, India, in July 2012. The 30 revised regular papers presented together with 10 short papers and 13 poster sessions were carefully selected from 135 submissions. The papers are organized in topical sections on VLSI design, design and modeling of digital circuits and systems, testing and verification, design for testability, testing memories and regular logic arrays, embedded

systems: hardware/software co-design and verification, emerging technology: nanoscale computing and nanotechnology.

FUNCTIONAL DESIGN ERRORS IN DIGITAL CIRCUITS

DIAGNOSIS CORRECTION AND REPAIR

Springer Science & Business Media Functional Design Errors in Digital Circuits Diagnosis covers a wide spectrum of innovative methods to automate the debugging process throughout the design flow: from Register-Transfer Level (RTL) all the way to the silicon die. In particular, this book describes: (1) techniques for bug trace minimization that simplify debugging; (2) an RTL error diagnosis method that identifies the root cause of errors directly; (3) a counterexample-guided error-repair framework to automatically fix errors in gate-level and RTL designs; (4) a symmetry-based rewiring technology for fixing electrical errors; (5) an incremental verification system for physical synthesis; and (6) an integrated framework for post-silicon debugging and layout repair. The solutions provided in this book can greatly reduce debugging effort, enhance design quality, and ultimately enable the design and manufacture of more reliable electronic devices.

ANALYSIS, ARCHITECTURES AND MODELLING OF EMBEDDED SYSTEMS

THIRD IFIP TC 10 INTERNATIONAL EMBEDDED SYSTEMS SYMPOSIUM, IESS 2009, LANGENARGEN, GERMANY, SEPTEMBER 14-16, 2009, PROCEEDINGS

Springer This book presents the technical program of the International Embedded Systems Symposium (IESS) 2009. Timely topics, techniques and trends in embedded system design are covered by the chapters in this volume, including modelling, simulation, verification, test, scheduling, platforms and processors. Particular emphasis is paid to automotive systems and wireless sensor networks. Sets of actual case studies in the area of embedded system design are also included. Over recent years, embedded systems have gained an enormous amount of proce- ing power and functionality and now enter numerous application areas, due to the fact that many of the formerly external components can now be integrated into a single System-on-Chip. This tendency has resulted in a dramatic reduction in the size and cost of embedded systems. As a unique technology, the design of embedded systems is an essential element of many innovations. Embedded systems meet their performance goals, including real-time constraints, through a combination of special-purpose hardware and software components tailored to the system requirements. Both the development of new features and the reuse of existing intellectual property components are essential to keeping up with ever more demanding customer requirements. Furthermore, design complexities are steadily growing with an increasing number of components that have to cooperate properly. Embedded system designers have to cope with multiple goals and constraints simul- neously, including timing, power, reliability, dependability, maintenance, packaging and, last but not least, price.

OUT-OF-ORDER PARALLEL DISCRETE EVENT SIMULATION FOR ELECTRONIC SYSTEM-LEVEL DESIGN

Springer This book offers readers a set of new approaches and tools a set of tools and techniques for facing challenges in parallelization with design of embedded systems. It provides an advanced parallel simulation infrastructure for efficient and effective system-level model validation and development so as to build better products in less time. Since parallel discrete event simulation (PDES) has the potential to exploit the underlying parallel computational capability in today’s multi-core simulation hosts, the author begins by reviewing the parallelization of discrete event simulation, identifying problems and solutions. She then describes out-of-order parallel discrete event simulation (OoO PDES), a novel approach for efficient validation of system-level designs by aggressively exploiting the parallel capabilities of todays’ multi-core PCs. This approach enables readers to design simulators that can fully exploit the parallel processing capability of the multi-core system to achieve fast speed simulation, without loss of simulation and timing accuracy. Based on this parallel simulation infrastructure, the author further describes automatic approaches that help the designer quickly to narrow down the debugging targets in faulty ESL models with parallelism.